REMARKS

Applicants thank the Examiner for the courtesy of participating in an informal telephone conference to discuss the status of the claims and the teachings of the prior art. Although no agreement was reached concerning patentability of the invention, Applicants did generally discuss with the Examiner the option of filing an RCE with a Preliminary Amendment and including amendments to the claims which would emphasize structural and operational differences over the prior art.

Claims 11-16, 17-22 and 32-37 were rejected under 35 U.S.C. 103(a) as being unpatentable over Asakura.

Claim 11 has been amended to focus the claim on the structure illustrated in Figure 16 of the application. More specifically, Applicants now claim "at least one discrete resistor having a resistive region obtained within said active area, the discrete resistor having first and second ends to which metal contacts are formed." Applicants further claim "the delimitation structure defining a width of the discrete resistor between the first and second ends." Applicants respectfully submit that Claim 11 now recites structural distinctions with respect to the teachings of Asakura.

The Asakura reference does not teach a discrete resistor formed in a wafer. The term "discrete" in this context is given its ordinary meaning of separate or distinct or not a part of as with respect to other components. The resistance identified by the Examiner is a parasitic resistance associated with a drain/source region of a transistor. This source or drain is not a discrete component, in this context, but is rather a part of the transistor component. Still further, the parasitic resistance in Asakura, because it is a drain/source region, does not have first and

second ends of a discrete resistor to which metal contacts are formed. Additionally, there is no teaching in Asakura for having the gate structure, which the Examiner asserts meets the claimed delimitation structure, define the width of the resistor between the first and second ends with metal contacts. In view of the foregoing, Applicants respectfully submit that Claim 11 distinguishes over the cited prior art.

Claim 17 has also been amended to focus the claim on the structure illustrated in Figure 16 of the application. Applicants claim "at least one resistor region within said active area, the resistor region having first and second ends to which metal contacts are formed." Asakura does not teach such a structure. Rather, Asakura teaches a parasitic resistance associated with a drain/source region of a transistor which does not have first and second ends with associated metal contacts. Applicants further claim a "delimitation structure defining a width of the resistor region between the first and second ends." Asakura does not teach this structure. Rather, Asakura teaches a gate structure which does not define the width of the rain/source region (resistance). In view of the foregoing, Applicants respectfully submit that Claim 17 distinguishes over the cited prior art.

In Claim 32, Applicants claim a "discrete resistor having first and second ends to which metal contacts are formed." Again, the parasitic resistance taught by the source/drain regions in Asakura is not a discrete resistor having first and second ends with associated metal contacts. Applicants still further claim that the delimiter structure defines "a size and shape of the discrete resistor," but does not comprise "a transistor gate structure of the integrated circuit." In Asakura, the delimiter identified by the Examiner is the polysilicon gate of a transistor whose source/drain regions are asserted to be resistive. Applicant specifically claims, to the contrary, that the

delimiter structure is not a gate structure of the integrated circuit. There is no teaching or suggestion in Asakura for the use of non-gate structures as discrete resistor delimiters. In view of the foregoing, Applicants respectfully submit that Claim 32 distinguishes over the cited prior art.

In Claim 33, Applicants claim a "delimitation structure on top of said active area that delimits a width of said resistive region." Applicants further claim "a pair of electrical metal contacts positioned at opposite ends of a length of the resistive region." There is no teaching or suggestion in Asakura for this specifically claimed width/length configuration of the resistive region as defined by the placement of the delimitation structure and metal contacts. In view of the foregoing, Applicants respectfully submit that Claim 33 distinguishes over the cited prior art.

In Claim 36, Applicants claim "a polysilicon structure, which is not a transistor gate structure of the integrated circuit, defining a mask which delimits a width of ion implantation which forms the resistive region." As discussed above, the teaching in Asakura is for the use of a polysilicon gate structure to delimit source/drain regions having a parasitic resistance. There is no teaching or suggestion in Asakura, however, for using non-transistor gate structure polysilicon delimiters for delimiting a width of ion implantation which forms a resistive region. In view of the foregoing, Applicants respectfully submit that Claim 36 distinguishes over the cited prior art.

Applicants respectfully submit that the application is now in condition for favorable action and allowance.

Respectfully submitted,
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